Rev.B

DRIVEPACK SERIES DP1

CIRCUIT DESCRIPTION AND SERVICE NOTES

The information in this document is intended for use by qualified, factory authorized Crown technicians.

WARNING! HAZARDOUS VOLTAGES PRESENT!

INTRODUCTION

These notes are intended to assist maintenance and service of the DP1 amplifier. Please refer to the following schematic diagrams and assembly diagrams while reading this document:
137084-4 PWA, DP1 PANEL
138037 DWG, ASM DP1 [#'s in square brackets refer to item # on dwg.]

The operation of the DPIP input module will be referred to where applicable to system operation and troubleshooting but the primary focus of this document is the amplifier itself. DSP troubleshooting will be provided in separate documents applicable to each of the 3 versions of DPIP modules, DPIP-AN, DPIP-CN, and DPIP-Basic.

This document consists of the following 4 sections:

A) Mechanical Construction
B) Circuit Description/Operation
C) Troubleshooting Tree
D) Service notes

MECHANICAL CONSTRUCTION

The mechanical structure of the amplifier comprises 3 main components: chassis/cover, front panels, and Internal PWA modules/Interconnects.

Excluding the DPIP, the Main Panel PWA contains all 6 of the submodule PWB's.

The one piece chassis incorporates the PWB mounting and acts as a heat sink as well as provide mounting for the DPIP input panel, power panel and rear cover. The junction between the chassis and panels as well as chassis and cover are sealed with flexible rubber gaskets in order to provide moisture resistance. **The gasket used on the DPIP panel is made of electrically conductive material required for ESD immunity and is light gray in color for differentiation from the black power panel gasket of the same size and shape.**

The internal PWB arrangement consists of 5 different sub assemblies as follows:

1) DPIP Input Module
2) Main Amplifier/SMPS Hi voltage switch mode power supply/Output and Misc. house keeping functions (clock, prop_vcc, current limit) hardwired to the Display.
3) LF Modulator
4) Speaker Interface
5) LVPS – Low voltage flyback power supply

The DPIP Input module is attached to the chassis via 4 8-32 screws. It is connected to the Main amplifier PWB through a 40Pin FFC 0.5mm ribbon cable [30]. The connector is a Molex ZIF Easy-On version with a cam-actuated latch. The latch is simply rotated in place upwards, the cable is inserted with the blue edge facing the latch side and the latch is then pressed down to secure it. Proper insertion can be observed by an evenly spaced 1/16” parallel gap between the top of the connector and the edge of the blue reinforcement. **This connection is the first item to check in the result of a failed unit, both at the amplifier and the DPIP**. The connection at the amp is secured with ~ 3/8” bead of RTV on the latch side from the factory. Vibration of the cable is minimized by a .75”x1”x.4” foam pad on the cable that is pressed between the DPIP PWB and the cover when the DPIP is inserted into the chassis. See Figure 1 for an example of a correctly inserted connection at the amp secured with RTV and Figure 2 for and example of a poorly inserted, misaligned cable.

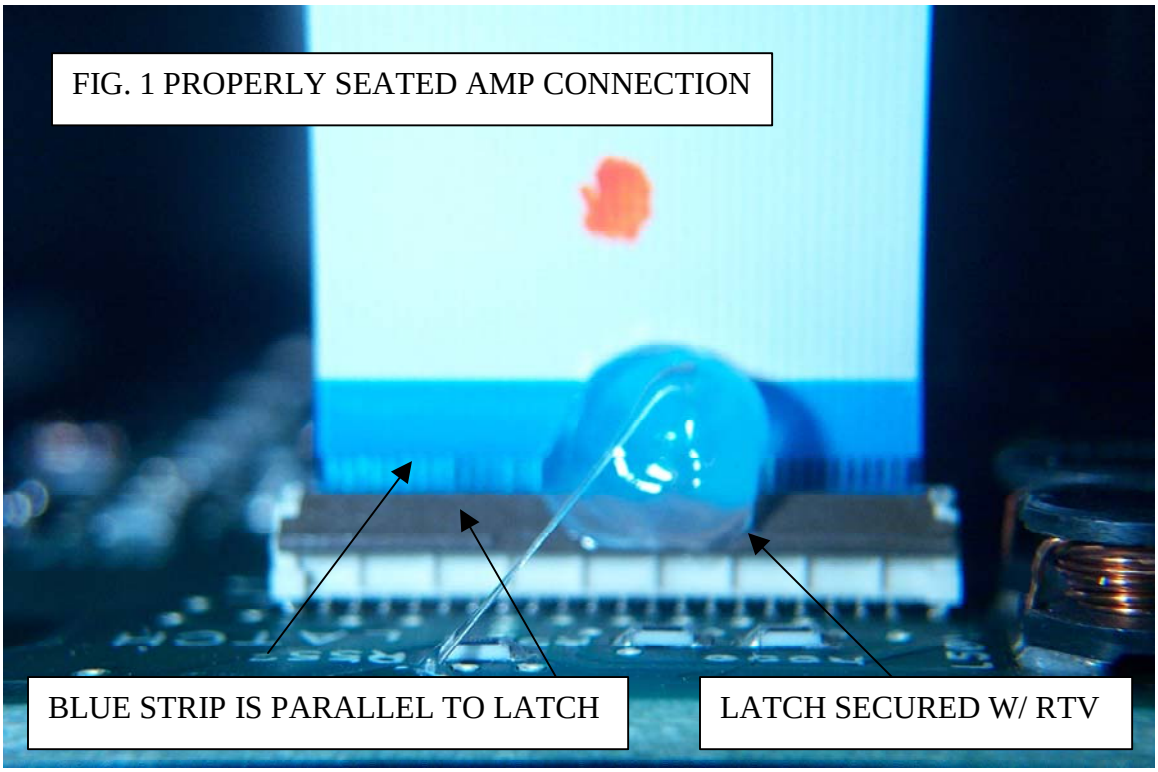


FIG. 1 PROPERLY SEATED AMP CONNECTION

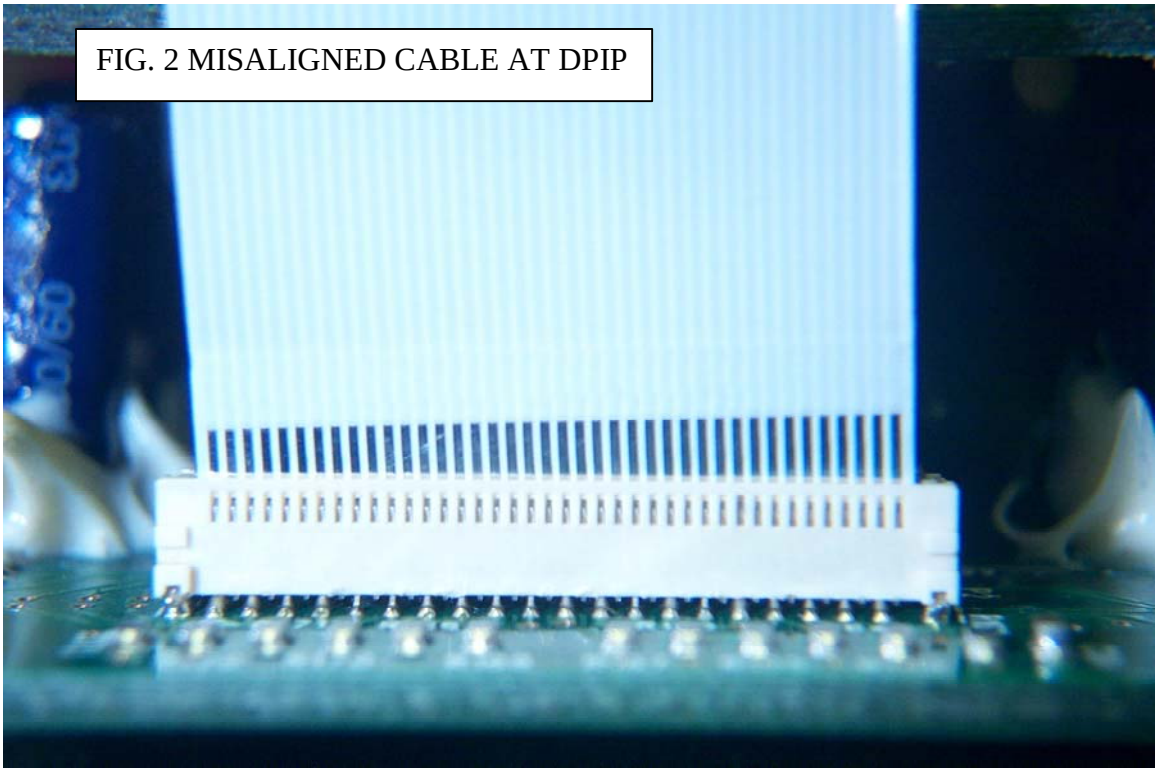


FIG. 2 MISALIGNED CABLE AT DPIP

A formed insulator [17] is placed into the chassis adhesive strips down, before any PWB's are attached. There are 2 X's on the insulator denoting the locations of self stick rubber bumpers [18] used for support of the Main power XFMR.

The Main Amplifier/SMPS/Output PWB is fixed to the chassis using 18 8-32x.312 screws [16] and 3 8-32x.375 screws where the shields are mounted. All of the TO-220 and TO-247 devices are attached to the chassis using the appropriate spring clips. There is a ceramic insulator used under each of these devices for electrical isolation from the chassis in addition to heat sink compound to transfer heat away from the device. **It is critical that the metal tabs of these devices do not touch each other to prevent shorting when installed or replaced. See Figure 3.**

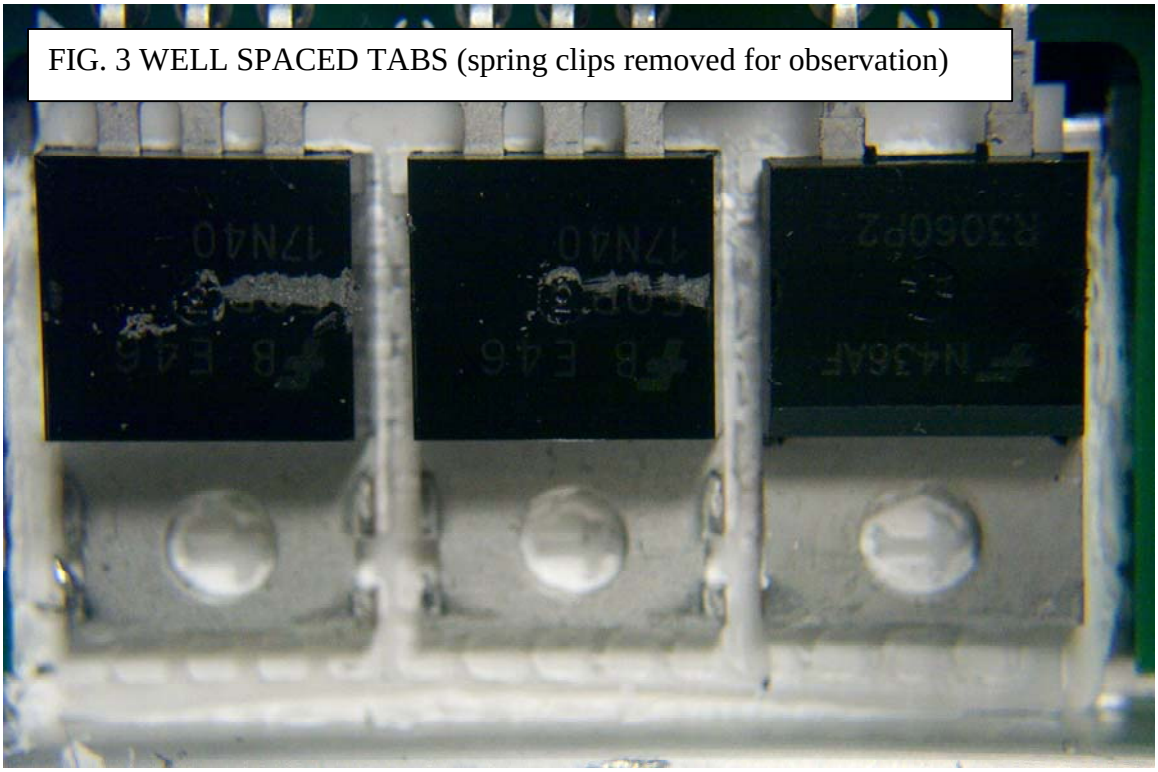
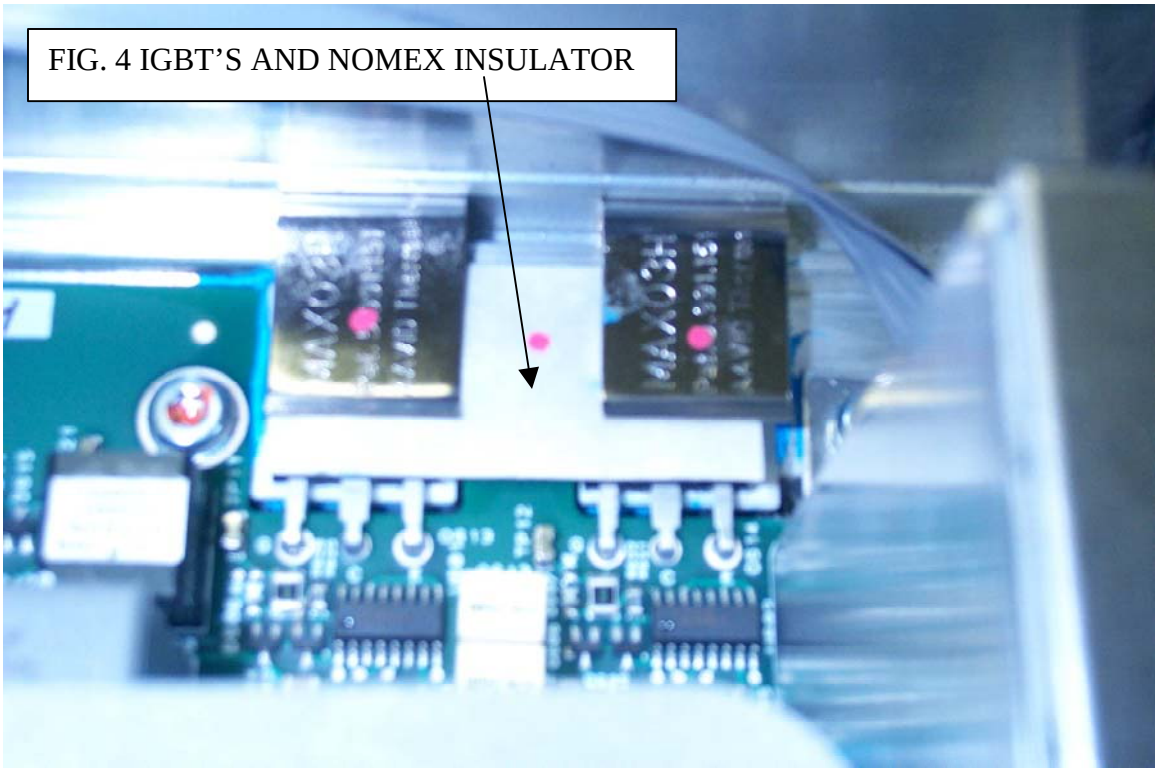


FIG. 3 WELL SPACED TABS (spring clips removed for observation)

The following is the recommended procedure for assembling the Main/SMPS PWA into the chassis to prevent stressing the device leads:

1) Apply a thin layer of Heat sink compound [43] to the land areas of the chassis under the power devices.
2) Insert the appropriate ceramic insulators and apply heat sink compound on top.
3) Insert Main PWB and SMPS PWB adjusting ceramics so that they are not trapped under the PWB's.
4) Install mounting screws. Assembly drawing specifies torque requirements.
5) Press spring clips into place allowing a small gap to inspect for device separation.

Alternately it is possible to replace single devices without removing the entire PWB by removing the spring clip, clipping the leads and unsoldering them. Then inserting a preformed part onto the re-gooped ceramic and resoldering from the topside. Care should be taken with this approach to ensure excessive topside solder does not form a bottom side short. **A 1.8"x.85" Nomex insulator [25] is placed over the IGBT's at Q613&Q614 before the clips are attached as a CSA regulatory requirement. See Figure 4.**



The Main and SMPS modules are both on the same PWA.

The LF Modulator PWA is plugged in perpendicularly to the Main PWB via dual row 30Pin right angle 0.1ctr header connector (P100). This board is held in place by a foam pad on the cover [415].

The Output filter is integrated into the Main/SMPS PWA.

The Speaker interface PWB is connected to the Output PWB via the speaker interface cable at P2001 (137485-1). The SPKR INTFC PWB is mounted to the cover with 4 6-32X.312 screws from the inside. The mounting holes are spaced to assure correct orientation.

The Low Voltage power supply PWB is plugged into the SMPS PWB at J600 similar to the way the Modulator is plugged into the Main. Several devices on the LVPS are mounted vertically to a heat sink plate (136844-1) with a clip and insulator. This plate is then covered with thermally conductive foam gap filler pad [38] which helps keep the module seated and transfer heat away from the LVPS to the cover. A small pink sill pad (133589-1) is inserted between the clip and body of U700 as a double insulation barrier as required by regulatory.

The Display PWB is flipped over and attached to the Power Panel (137758-1) using 2 6-32x .312 screws. A 4-pin ribbon cable (138396-1) hardwires the Display PWB to the Main PWB at P1000-J1000.

The PowerCon inlet (Blue) [5] and PowerCon outlet (Grey) [3] connectors are also mounted to the Power panel using 4 M3x8 flathead screws [4]. These are wired to the main at W1A,W1B (**L**ine – Brown Leads) and W2A,W2B (**N**eutral – Blue leads) as marked on the connectors. The GRN/YEL ground leads are attached directly to the chassis via 2 8-32x.312 screws into ring terminals.

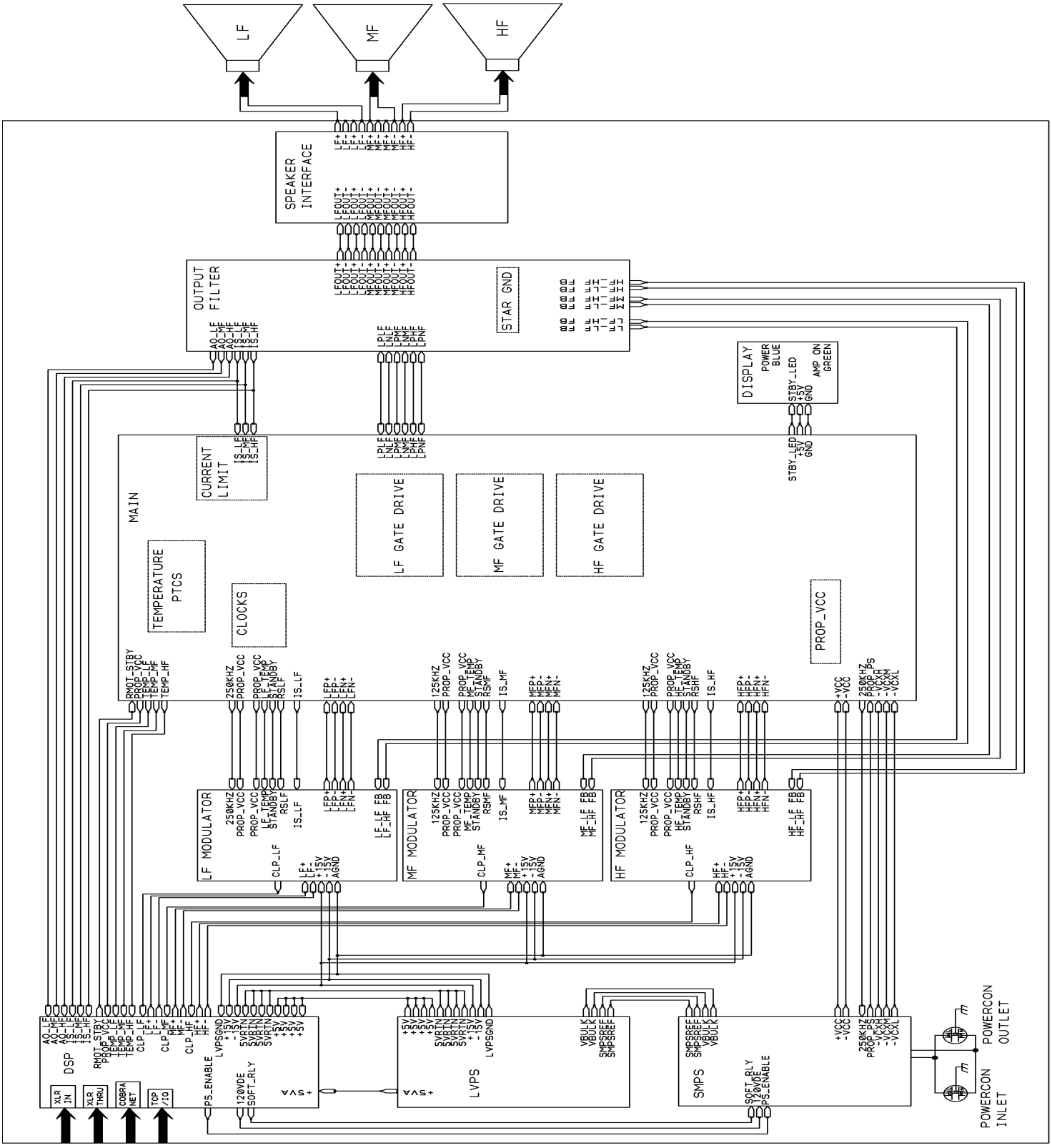


FIG. 5 DRIVEPACK BLOCK DIAGRAM

CIRCUIT DESCRIPTION/OPERATION

DPIP

Its purpose is to provide input signal processing, gain, crossovers, equalization, delay, output limiting and controls power-up/power-down sequencing as well as monitor amplifier parameters such as rail voltage, output voltage, output current, channel clipping, heat sink temperature and report fault conditions. The DPIP is responsible for controlling the soft start relay, making the 120V/240V operation decision, enabling the Hi voltage power supply and putting the amp in ready or sleep state. The DPIP is powered exclusively by the 5V and +/-15V supplied by the LVPS. This allows the DPIP to maintain communications through the network in the event of a power amp or SMPS failure.

This amp has no external power switch. Power is applied by inserting the power cord into the PowerCon connector and twisting it clockwise. The unit is configured to start in 240V mode.

Input Module Processing (Minimum required control and signal processing)
Power-up Sequencing
The input module is an integral part of the power-up sequence. It is responsible for the soft-start of the main supply as well as deciding if it is necessary to change to the 120V mode. The input module will also decide when to start the main supply and when to shut it down. The following sequence must be implemented by the input module every time the low voltage supply is applied. See Figure 6 for a flow diagram.

Initial Power Sequence (when power supplies are applied to module)

Step 1. Delay 0.1 to 0.3 seconds including the initialization time of the module.
Step 2. Disable the soft-start relay by setting SOFT_RLY high.
Step 3. If the power setting is set to on continue to the Enable High voltage supply sequence.

Enable High Voltage Supply Sequence

Step 1. Wait for the Proportional VCC to drop to less than 1.3 VDC. (Discharges the VCC supply if recently powered up to properly determine if voltage doubler is needed.)
Step 2. Enable the soft-start relay by setting SOFT_RLY low.
Step 3. Delay for 25 milliseconds.
Step 4. Enable the high voltage supply by setting PSENABLE high.
Step 5. Delay for 0.1 second for high voltage supply to stabilize.
Step 6. Disable the soft-start relay by setting SOFT_RLY high.
Step 7. Delay for 0.1 seconds.
Step 8. Verify the supply is operating by measuring the voltage of the PROP_VCC. If not greater than 1.4 VDC disable the high voltage supply and display and / or report a power supply error.
Step 9. Measure the voltage of the PROP_VCC signal to test if the voltage doubler is necessary. If PROP_VCC is greater than 2.6 VDC (amplifier assumed to be

plugged into 240V line) go to step 18.

Step 10. Enable the soft-start relay by setting SOFT_RLY low.

Step 11. Delay for 25 milliseconds.

Step 12. Disable the high voltage supply by setting PSENABLE low.

Step 13. Enable the voltage doubler by setting the 120VDE signal high. Note: The state of the 120 VDE signal does not change after this point regardless of subsequent changes to the power setting.

Step 14. Enable the high voltage supply by setting PSENABLE high.

Step 15. Delay for 0.1 seconds.

Step 16. Disable the soft-start relay by setting SOFT_RLY high.

Step 17. Delay for 0.1 seconds.

Step 18. Measure the voltage of the PROP_VCC signal to test for proper high voltage supply operation. If PROP_VCC is greater than 3.5 V (nominal = 4 V) continue. If PROP_VCC is less than 2.8 V then the power supply is not properly functioning. Shut down the high voltage supply by setting PSENABLE low and display and / or report a power supply error.

Step 19. Delay for 0.5 seconds to allow the high voltage supply to charge up.

Step 20. Enable the amplifier output channels if desired by setting the RMOT_STBY signal high. Audio signals may now be applied to the LF, MF, and HF inputs.

Subsequent High Voltage Supply Sequence

If the state of the power setting is changed from off to on after the Enable High Voltage Supply Sequence is completely executed this shortened sequence is used to reapply the high voltage supply.

Step 1. Enable the soft-start relay by setting SOFT_RLY low.

Step 2. Delay for 25 milliseconds.

Step 3. Enable the high voltage supply by setting PSENABLE high.

Step 4. Delay for 0.1 second for high voltage supply to stabilize.

Step 5. Disable the soft-start relay by setting SOFT_RLY high.

Step 6. Delay for 0.1 second.

Step 7.Enable the amplifier output channels if desired by setting the RMOT_STBY signal high. Audio signals may now be applied to the LF, MF, and HF inputs.

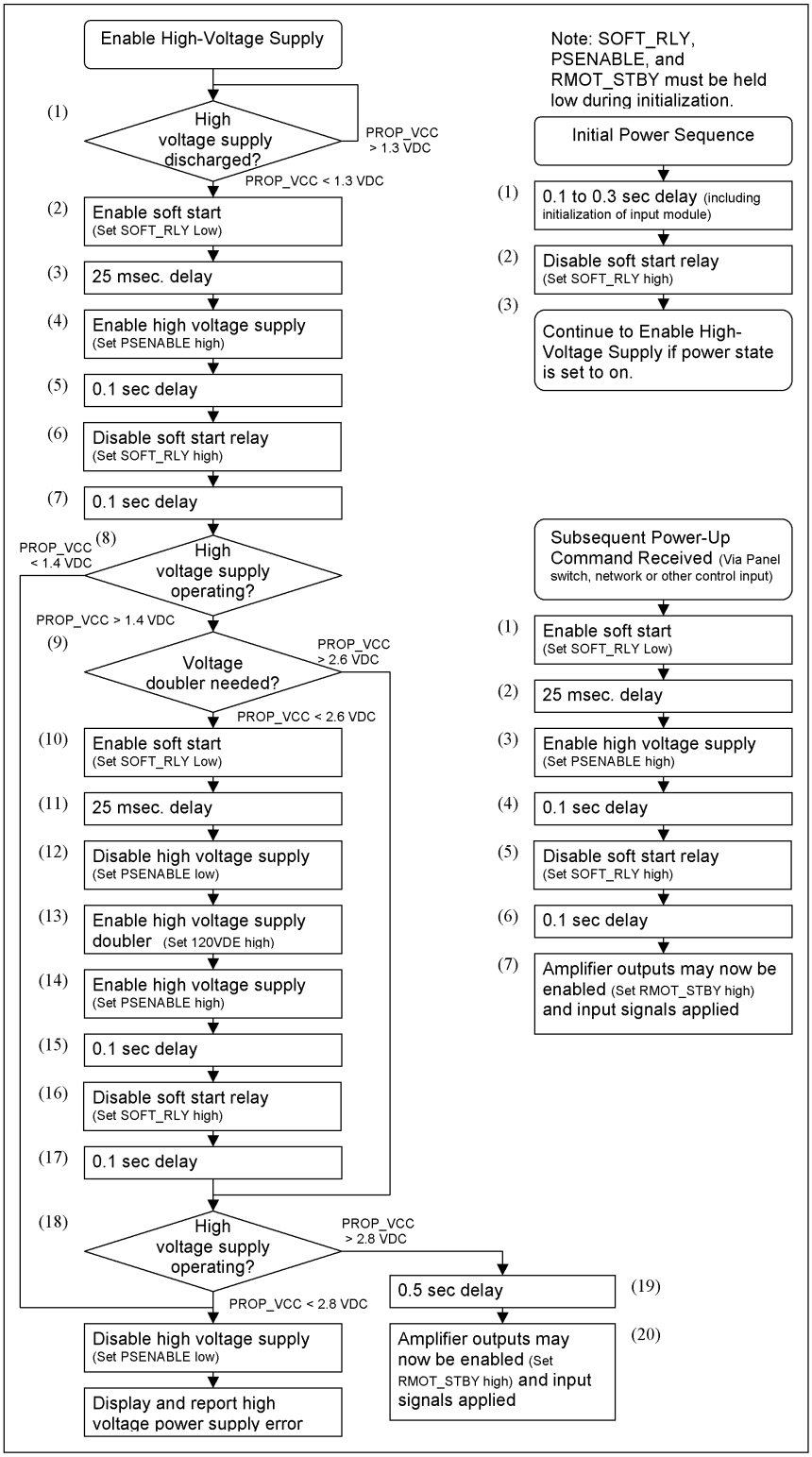


Figure 6, Power-Up Sequence
(Numbers in brackets refer to step numbers in section 0)

Power-Down Sequencing

The following sequence must be implemented by the input module for power-down. See Figure 7 for a flow diagram.

Step 1. Mute the audio signals into the LF-, MF- and HF- inputs.

Step 2. Place the amplifier output channels in standby by setting the RMOT_STBY signal low.

Step 3. Disable high voltage supply by setting PSENABLE low.

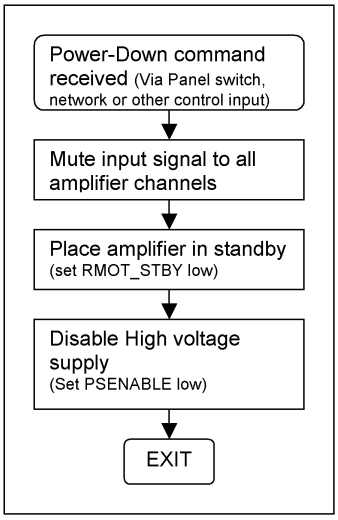


Figure 7, Power-Down Sequence

Sleep Mode

The input module is required implement an auto sleep feature. The input signal is monitored and compared to a threshold level of –78dBu FS. If the input signal is below the threshold for more than 120 minutes the input module will disable the amplifier by setting RMOT_STBY low. When the input signal rises above the threshold the input module will immediately set RMOT_STBY high.

Brownout control

The input module is required to set ROMT_STBY low if the proportional VCC drops bellow 2.8 VDC and return it back high if proportional VCC returns above 3.0 VDC. The input module must keep ROMT_STBY low for a minimum of 0.5 seconds before attempting to return it high.

Over-voltage control

The input module must set ROMT_STBY low if proportional VCC exceeds 4.9 VDC and return it high if proportional VCC falls below 4.9 VDC.

FAILURE MODES: The primary failure of DPIPS has been due to improper connection of the DPIP cable causing a short between +5 and –15V or +15V lines which results in blown tantalum capacitors C177 - 6.3V 47UF or C150, C153 – 16V, 10UF.

MODULATOR

Reference designators for the LF are 100's and 200's.

Due to the limited frequency response of the LF channel (20Hz-2Khz) the LF modulator operates at 62.5Khz.

The Modulator performs the balanced to single-ended conversion of the input signal from the DPIP. See U100-A. From here the signal goes to the Error amp at U101-D and is combined with Low frequency and High frequency feedback from the output via LF_LF FBC and LF_HF FBC to remove the 2^{st} and 4^{rd} harmonics of the switching frequency. This is tuned out by the traps at R104 and R109. This tuning is set during modules functional testing, fixed with orange torque seal and is not service adjustable. The error amp then feeds a window comparator formed by U102-A and U102-B to generate the clip indicator CLP_LFC. (The DPIP monitors CLP events vs. time and will respond with a command to limit the output if excessive clipping is detected). U103-D forms a clamp of the error amp driven by STANDBYC. This prevents the error amp from slamming to the rails during a system mute. The error amp signal is then compared to a reference triangle wave in order to produce the pulse width modulation driving the amplifier switches.

There are several inputs to the triangle wave generator which affect the timing of the modulation. Proportional rail voltage (PROP_VCC), Low Frequency output feedback (LF_LF FB), Output current sense (IS_LF) and Temperature (LF_TEMP_LF) are used to dynamically control the DC level of the triangle wave. The primary adjustment of the modulators is the setting of the Static UL/OL (Underlap/Overlap) R193 potentiometer. This is similar to a bias adjustment and is performed under a no load condition at nominal 120V line. See Figures 8,9,10 of Output Filter Board section for examples of Ideal, Underlapped and Overlapped conditions. In general the trade off is distortion vs. heat dissipation. An underlapped channel will run cooler but have higher distortion vs. an overlapped channel that runs hotter with lower distortion.

The error amp signal and triangle wave reference are summed into the comparators at U104 and U105, buffered by AND gate U106 resulting in 2 sets of 62.5kHz square waves LFP+C,LFP-C and LFN+C,LFN-C gate drive signals to the power amp FETs. The output of gate drives is controlled by the RSLFC. This signal can turn off the gate drive due to current limit and under-voltage lockout (See Main). E101 is a Green test LED which is lit when the amp has been enabled.

TP101 is the output of the error amp. With no input signal the error amp should be 0V +/- 100mVDC. TP102 is the triangle output. The LF channel will be a 62.5kHz triangle wave 10V pk-to-pk. TP105 is AGND. The PWM outputs of the modulator (LFN+C, LFN-C, LFP+C, LFP-C) are 62.5kHz square wave for the LF 50% duty cycle 5V +\- .25V.

FAILURE MODES: The Modulator board is signal level, low power and not prone to failure. No systemic failures of the modulator boards have ever been encountered.

MAIN AMP CHANNEL

The PWM output from the modulators is fed into each of the main amp channels at R200, R201 and R229, R230. The gate drive translator circuit built around U200 and U201 with associated BJT transistors that converts the GND referenced PWM signals of the modulators into +/-VCC referenced gate drive for the switching FETs. The gate drive translator circuit is self-powered via a charge pump made up of C210, C212, L200, D202, D205, D206, R216, R213, R214 and regulated via zeners D207 and D208 for the VP node. The gate drive circuitry is powered from the switching of the LP and LN coils.

The output of each amp channel is the highpower PWM signals VPLF and VPLN that are fed to the output filter coils. These signals will be switching in unison at the channel switching frequency (62.5kHz LF) as a square wave with pk-to-pk amplitude of 205V.

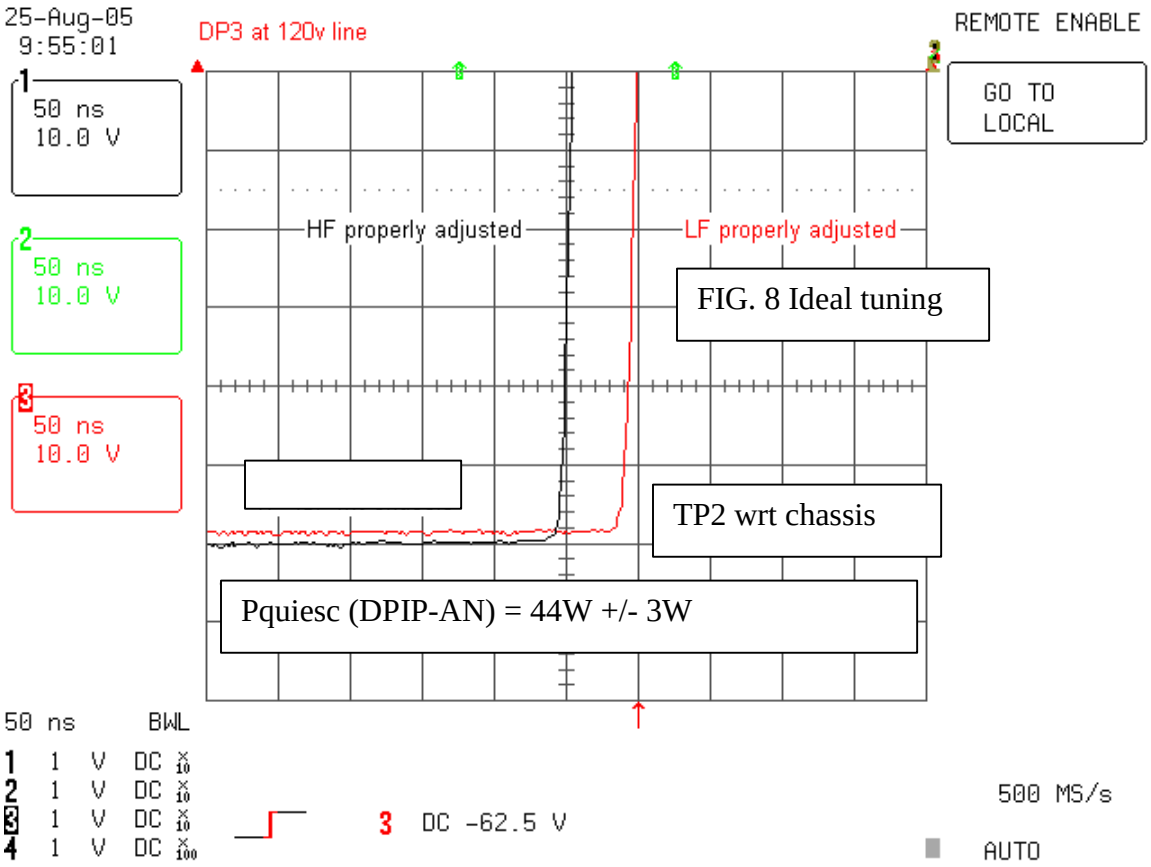
FAILURE MODES: Common failures observed in the main amp channels are shorted FET's and Diodes, which can be determined with a diode check of a DMM. Typical values for diodes D201A-D201D are 0.37V. Typical values for the FETs Q208, Q209, Q218, Q219, Q222, Q223, Q226, Q227 are 0.65V S-G and .37V S-D. Secondly all BJT's should be diode checked in the gate drive circuitry. Third all the low Z gate drive resistors should be ohm'd out before applying power as they can fail opened when FET's get blown. Lastly the Gate Drive IC's U200-U201 should be replaced if no other problem is found.

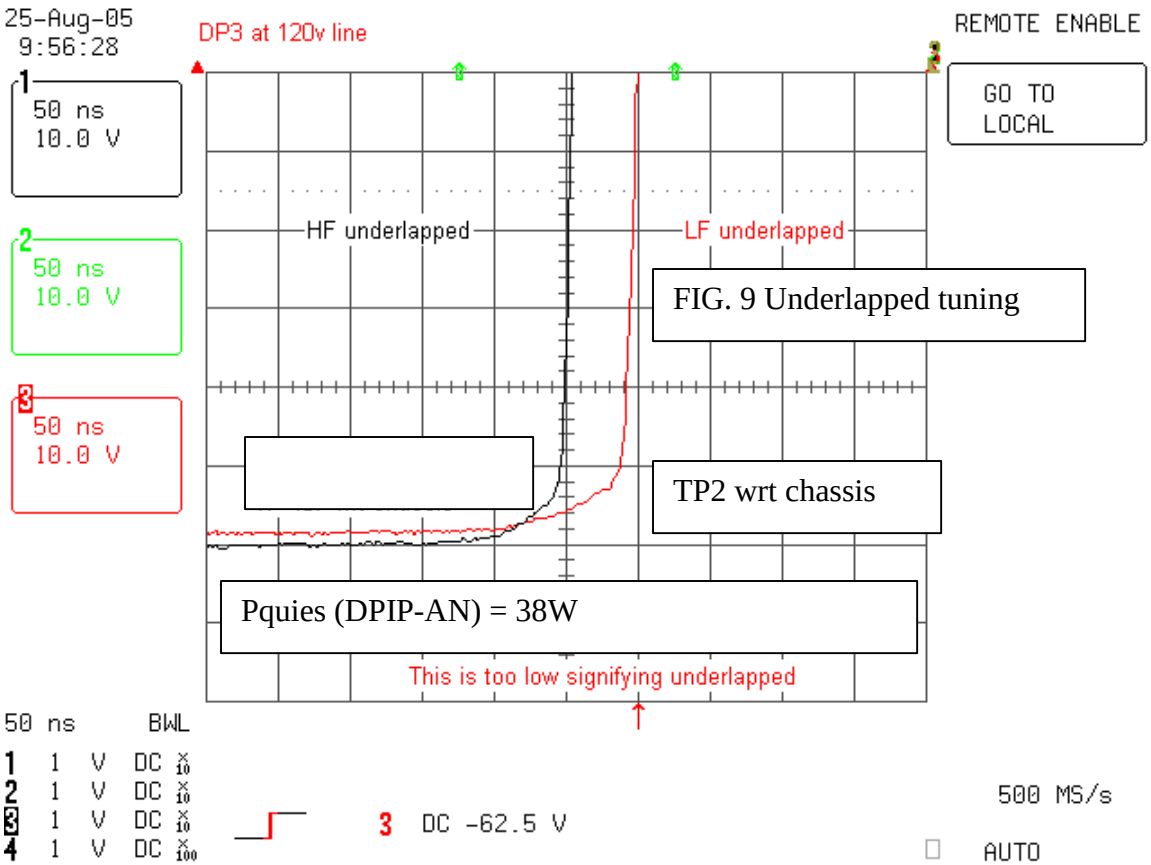
OUTPUT FILTER

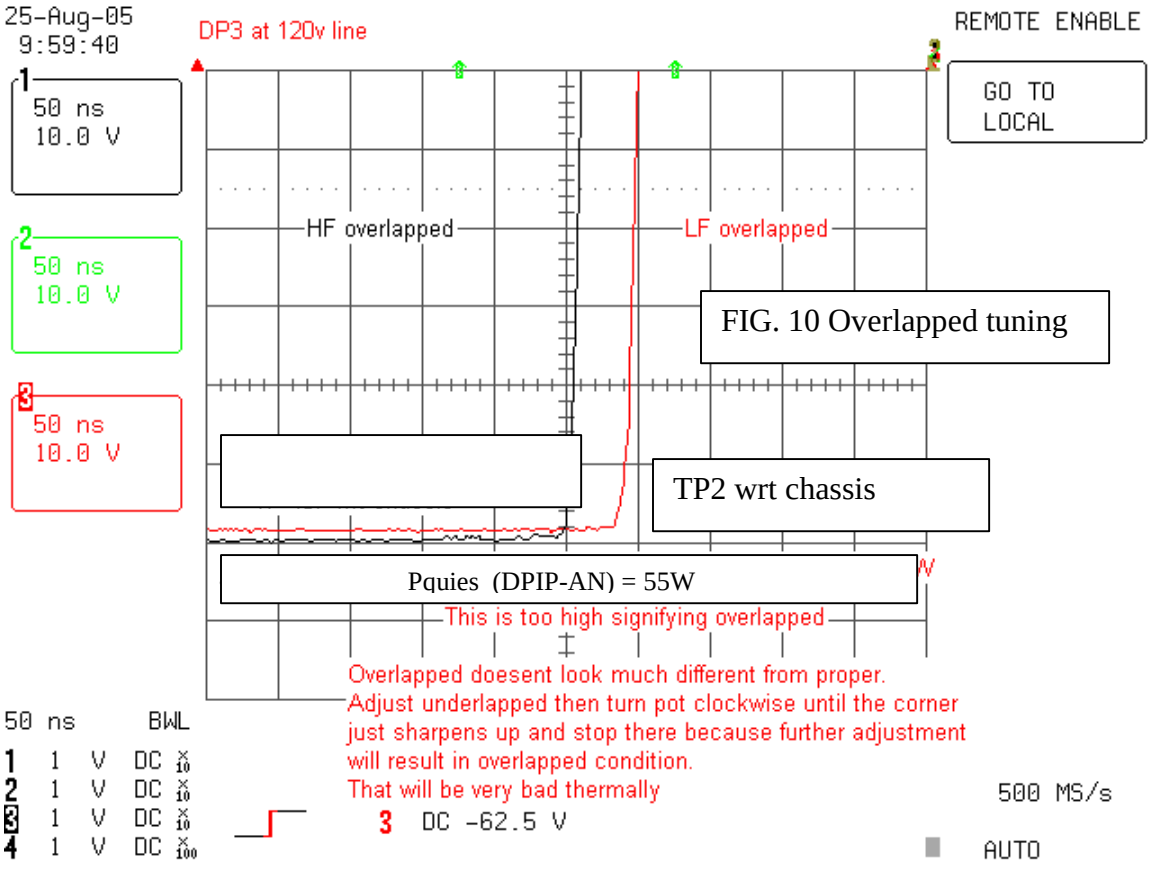
The currents from the VP and VP nodes are summed together through the Power inductors of the output filter (LP1-A, LP1-B).
The signal for each channel then goes through a series of filters and traps to clean up the signal and remove the noise at the switching frequency. The low frequency portion of the signal is used as LF feedback for the modulators via LF_LF_FB and HF_LF_FB. The only active circuitry on the output board is the signal conditioning op-amp U506. This provides real-time scaled monitoring of the output voltage and current of each channel. AO_LF is the voltage and IS_LF is the current. Scaling is 9.68mV/V for AO_LFB and 31mV/A for the LF_IS. The most common failures to date on the output filter have been failure of the vertical cement current sense resistors. In some cases involving high vibration, the leads have fractured resulting in a higher than normal impedance when measured. This results in premature current limiting when driving a load. Hi temp epoxy is used to secure these and repair is most difficult. The next most common failure observed has been the terminals in the Molex connector to the speaker interface board. Sometimes the terminals can get pushed out of the housing or damaged resulting in no output. Care should be taken when installing the cover to avoid pinching the speaker interface leads between the cover and shield.

FAILURE MODES: High strength epoxy under the coils makes individual coils replacement unlikely. **Whenever this is done, it is critical to readjust the OL/UL settings on each individual modulator board for optimal performance.** The test points for setting OL/UL is TP2.

Figures 8,9,10 for OL/UL adjustment. (Only LF trace applies to DP1)




25-Aug-05
9:56:28
DP3 at 120v line
REMOTE ENABLE
1
50 ns
10.0 V
2
50 ns
10.0 V
3
50 ns
10.0 V
GO TO
LOCAL
HF underlapped
LF underlapped
FIG. 9 Underlapped tuning
TP2 wrt chassis
Pquies (DPIP-AN) = 38W
This is too low signifying underlapped
50 ns BWL
1 1 V DC
2 1 V DC
3 1 V DC
4 1 V DC
3 DC -62.5 V
500 MS/s
AUTO


25-Aug-05
9:59:40
DP3 at 120v line
REMOTE ENABLE
1
50 ns
10.0 V
2
50 ns
10.0 V
3
50 ns
10.0 V
GO TO
LOCAL
HF overlapped
LF overlapped
FIG. 10 Overlapped tuning
TP2 wrt chassis
Pquies (DPIP-AN) = 55W
This is too high signifying overlapped
Overlapped doesent look much different from proper.
Adjust underlapped then turn pot clockwise until the corner
just sharpens up and stop there because further adjustment
will result in overlapped condition.
That will be very bad thermally
50 ns BWL
1 1 V DC
2 1 V DC
3 1 V DC
4 1 V DC
3 DC -62.5 V
500 MS/s
AUTO

Measuring the real power draw is another good check to determine if the system is adjusted and operating correctly. By using the scope math functions to determine the real power draw based on the mean of RMS line voltage times RMS line current the table below lists approximate power draw value ranges for 3 different operating conditions using each of the 3 DPIP modules:

TYPICAL POWER DRAW AT 120VAC LINE FOR VARIOUS CONDITIONS

	DBX DPIP	CROWN AN	CROWN CN
SMPS OFF – AMP OFF =	9 ±3W	12 ±3W	16 ±3W
SMPS ON – AMP OFF =	22 ±3W	24 ±3W	27 ±3W
SMPS ON – AMP ON =	41 ±3W	44 ±3W	47 ±3W

SPEAKER INTERFACE BOARD

This PWB serves as the interface between the amp and speaker enclosure. It contains no active circuitry. EMI is controlled by a few small capacitors and resistors, which filter out the high frequency EMI and prevent it from reaching the output.

FAILURE MODES: Care should be taken when reassembling the cover to ensure that the wires of the SPKR INTFC cable do not get pinched between the tall cement block resistors of the output board and the bottom side pins of the Molex connector on the SPKR INTFC board.

DISPLAY BOARD

The Display board is mounted upside down to the power panel with both Blue and Green LED's.

The Blue LED indicates power is applied and will light immediately after the unit is plugged in. The Blue LED is powered from the 5V supply of the LVPS and not the SMPS Hi voltage supply.

The Green LED is controlled by the STNDBY line from the DPIP. During a normal power up sequence the Green LED will start flashing for approximately 4 seconds after power is applied then go solid. The Green LED indicates that the high voltage SMPS is up working and that the amp has been enabled.

FAILURE MODES: The most common failures observed with the Display board are busted LED's or busted pins on the display cable.

LVPS

The LVPS is a multiple output flyback converter driven off the rectified primary line voltage VBULK to SMPSREF typically 340VDC. It provides the following outputs:
5V @ 2A
+15V @ 300mA

-15V @ 200mA
The LVPS is regulated off the 5V line through the U701 reference and U704 optocoupler. The +/- 15V lines use linear regulators U703 and U702. The LVPS is controlled by the Viper100A U700 that is powered from an auxiliary winding of the flyback transformer. The Viper will free run at startup within the range of 78-82kHz. Once the +5V, +15V and –15V supplies are up, the clock circuit is powered and the timing is synced via U706 flip-flop and U705 optocoupler at 62.5kHz. Zeners D705 and D707 provide transient protection for the Viper during startup. A soft-start function is performed by R718, C726 and R703, C702.

Green LED E701 is lit when the +5V supply is on.

FAILURE MODES: The most common failure observed with the LVPS is opened SMT fuse F3 due to a bad DPIP connection. Less often, failures have resulted from solder bridging between Pins 1-2 and 4-5 of the Viper control IC U700. The device should be up off the board .020-.030" such that the 2 outside leads clear the solder fillets of the adjacent leads. In the rarest case where U700 has actually been damaged it is important to check the snubber diode D704, and zener clamp diodes D707&D705 as well as the series resistors R714 and R713.

SMPS

The SMPS hi voltage power supply is a self-resonant unregulated switch mode power supply. The supply includes a soft start feature and automatically detects line voltage for operation in either of 2 input voltage ranges: 100- 120VAC and 220-240VAC.

Soft start is controlled by the DPIP via relay K600 thru the SOFT_RLY signal. Initially a 6 ohm PTC RT600 is inserted in the line to limit inrush current. When the SOFT_RLY signal goes high, the relay is energized and the PTC is bypassed allowing full power operation. After initial charging of the primary bulk capacitors the relay is disabled and the PTC is bypassed. If the K600 relay fails the PTC will continue heating up until the current is limited so much that the unit ceases to function and shuts off. This is usually apparent by the hot smell of the PTC.

Voltage selection is accomplished via the voltage doubler relay K601 and also controlled from the DPIP thru the 120_VDE signal. Initially the SMPS start up in 240V mode with the relay disabled. The supply is enabled and the DPIP examines the PROP_VCC_DSP signal to determine if the +/- VCC rails are correct. If not the 120_VDE signal goes high and the voltage doubler relay is enabled. See DPIP power up section for more details.

The SMPS is synced at 250kHz thru the UC3846 PWM control IC. The resultant gate drive signals DRIVE_A and DRIVE_B are coupled by the gate drive transformer T600, buffered by U601-U602 and drive the IGBT's Q613 and Q614. See Figure 11 for a plot of the expected gate drive waveforms. The switched output of the IGBT's is fed into the resonant tank formed by C620 and L902. This tank is then fed into the main power transformer T601.

There are 2 fuses in the SMPS. F1 is the Main fuse rated at 20A. F2 is the resonant fuse rated at 12.5A. F1's purpose is to protect the IGBT's. F2's purpose is to protect the main XFMR. The full wave rectified output of the main xfmr is the amp rail voltage +/-VCC and will measure +/- 130VDC.

Another low power bridge is tapped off the secondary of the main xfmr formed by D616-D620 to generate the –VCXH and –VCXL voltages (-185V when the amp is on) used as the COM reference of the amp gate drive IC's U200, U201 in the gate drive translator circuit. See Main. Green LED E601 is lit when the SMPS has been enabled.

FALURE MODES: In general the supply will be working if the IGBT's are switching at 125kHz, 12V square wave as observed with a differential probe from G-E of Q613 and Q614. **A differential probe must be used because the SMPSREF is floating with respect to ground. When repairing the SMPS it is important to verify the IGBT switching waveforms while powered via external +5V and +/-15V supplies. Do not attempt to test the SMPS under full power line voltage until these waveforms have been verified.** IGBT's usually fail catastrophically and busted silicon is evident under the nomex insulator.

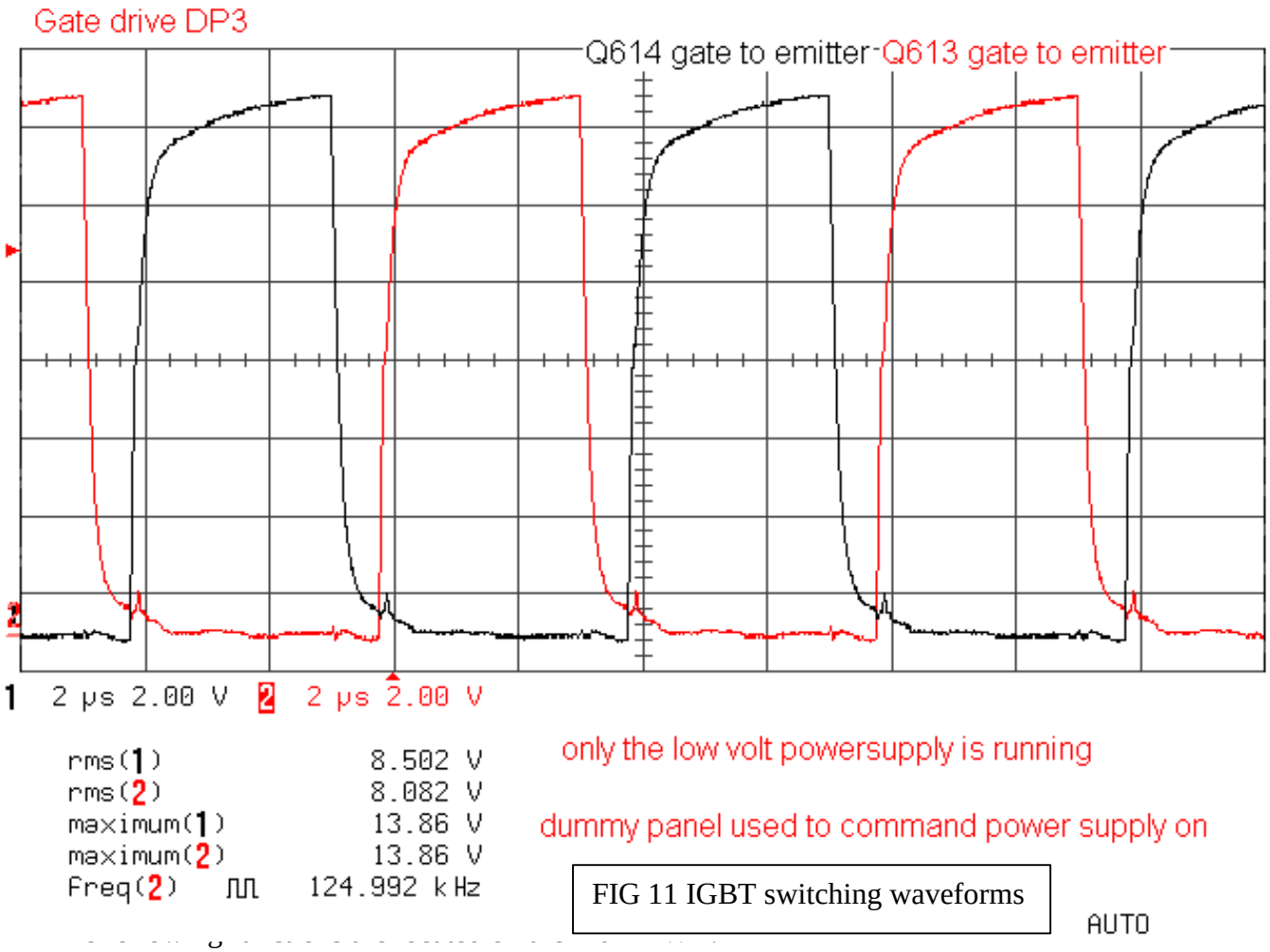


FIG 11 IGBT switching waveforms

CLOCKS – All clock signals are derived from Y500 a 4MHz oscillator buffered by U501 NOR gate. The LF modulator uses 125KHZ, 250_KHz is used by the SMPS and LVPS Sync.

CURRENT LIMIT – Independent cycle-by-cycle current limiting is implemented on each channel. The output current is detected from the Output board current sense resistors R321, R322 for the LF_IS. The current limit is scaled such that under normal operation is should never be hit. The current limit function is intended to prevent amp failure due to a shorted speaker. LF current limit is scaled at 0.031V/A and will trip the RSLF reset to the modulators at 45A.

TEMPERATURE MONTOR – Chassis temperature is monitored via 2 PTC 20K resistors RT1 and RT2. Heat from the chassis is transferred via the nearby standoffs from opposite sides of the chassis and reported to the DPIP via TEMP_HF (J1-19) and TEMP_LF (J1-18).
Scaling of the temperature signals is linear from 0V@ 30C to 5V@100C.

STANDBY – This signal is used to put the amplifier into standby. It is driven from 2 separate sources. 1) REMOT_STBY (J1-33) command from the DPIP active low. 2) Under voltage lockout from the PROP_VCC_DSP signal. This is done to prevent damage caused by attempting to switch the amp FETs with insufficient gate drive caused by low rails. This occurs when the Rails fall below +/-90V.

PROP_VCC_MOD – (TP500) is a scaled representation of the +/-VCC rail voltage. It measures 5V nominally for +VCC=130V and –VCC=-130V unloaded. This is used by the modulator to control the DC level of the reference triangle wave.

PROP_VCC_DSP (J1-20) – This signal is similar to the PROP_VCC_MOD signal above in that it is a scaled representation of the +/-VCC rail voltage. It is scaled for 4V nominal and responds much faster to changes in the rail voltage. It is derived directly off the secondary winding of the main power transformer T600, half-wave rectified by D621 and divided down through the divider formed by RR619, R620 and R621 as PROP_PS. It then is RC filtered and buffered at U500C. This signal is used by the DPIP to determine if the voltage doubler should be enabled.

TROUBLESHOOTING TREE

SYMPTOM	CAUSE	NEXT STEP
NO BLUE LED	Bad DPIP connection	Inspect and reconnect
	Blown LVPS fuse F3	Replace
	Busted LED	Inspect
	Busted display cable P1000	Replace
	Bad connection at PowerCon	Check continuity

	Bad LVPS	Replace LVPS
	Blown Main Fuse F1	Replace
	Burnt DPIP cable	Replace cable and LVPS fuse F3.
NO GREEN LED	Bad DPIP connection	Inspect and reconnect
	Blown resonant fuse F2	Check IGBT's
	Bad SMPS	Check +/- VCC from TP600 to TP602
		Verify IGBT switching 0-12V 125kHz square wave G-E w/ Diff probe
		Check SMPS diodes
	VCC low by 1/2	Verify K601 doubler relay enabled
	Load short	Check for shorted FETs
	Busted LED	Inspect
	Busted Display cable P1000	Replace
GREEN LED FLASHES BRIEFLY	SMPS Not running	Check Fuse F2
	VCC low by 1/2	Verify K601 doubler relay enabled
NO OUTPUT	Broken speaker interface conn	Inspect end of 6P Molex on P2001 for loose terminals.
OUTPUT DISTORTION	Premature current limiting caused by bad current sense resistor	Measure cement block 5W resistors on O/P PWB, LF= HF = .005 ohms
	Busted SMPS diodes	Lightly pull leads of D608-D611
DC OFFSET	Bad electrolytic dc blocking caps	Replace C168-169,C368-369

SERVICE NOTES

WHAT TO CHECK FIRST

40 Pin Cable at DPIP and SMPS-MAIN connection – A burnt conductor down the center of the ribbon cable is typically the result of an improperly connected DPIP.

Vp/Vn Switching – Check both nodes for square wave output
OL/UL – retune when swapping Outputs, Modulators and FETs
Fuses – F1 - Main, F2 -resonant tank, F3 - LVPS
FETs Open/shorted
IGBT switching
Spkr interface cable terminals – If Vp/Vn switching and no output, sometimes the terminals in the 10Pin Molex can get dislodged
+/-VCC = 260VDC from TP614 and TP615 to chassis.
VBULK/SMPSREF – Is the full wave bridge rectified output from TP600 to TP602 and should read +340V. If it is only measuring ½ that it is an indication that K601 the voltage doubler relay has failed or not been enabled.
With the use of a Crown DPIP-AN/CN module with network connectivity, errors can be traced by looking at the error messages reported on IQWIQ/SYSTEM ARCHITECT.
When encountering a failure the easiest first step should always be swapping in a known good module for the failed one to help isolate the problem. **It is important to retune the OL/UL setting for all channels when replacing FET's, Output PWB and Modulators.**

DRIVEPACK AMPLIFIER DP1 COMMON FAILURES

When encountering a failure the first step should always be swapping in a known good module for the failed one to help isolate the problem to the faulty PCB. Although the DrivePack Series Amplifiers are very reliable, we have noticed some common failures that are quick and easy to repair.

No power Blue LED illumination indicating no initial power.

- Check F1 and Q613, 614 on power supply PCB.
- Open connection of AC Power

No Green LED illumination (no high voltage rails)

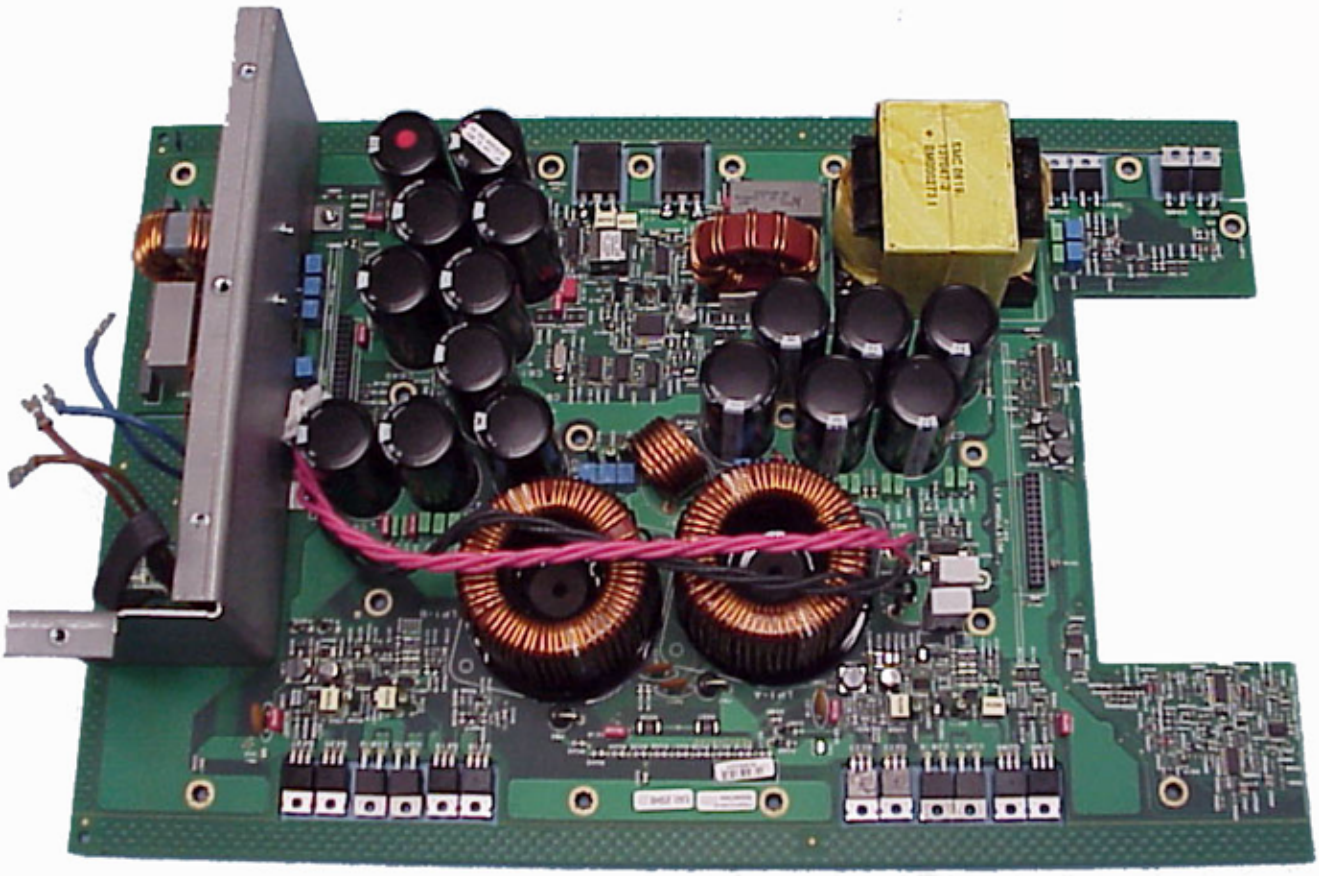
- Input module is defective
- Input module is good but is detecting some fault not allowing the voltage rails to energize
- The low voltage supply card is defective
- Fuses--F2-resonant tank fuse is open, F3 – LVPS fuse is open
- FET output transistors Open/shorted

No sound or noise

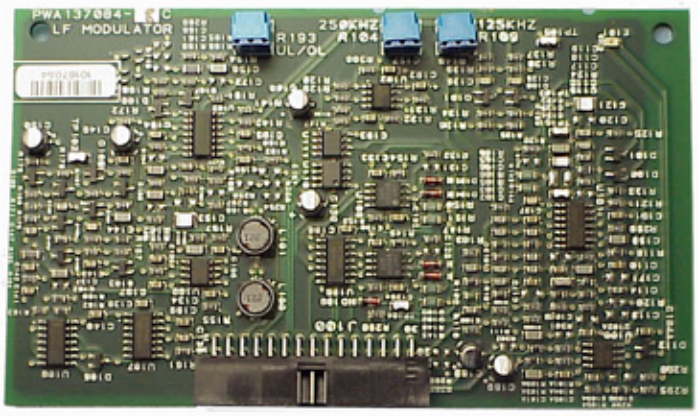
<u>This could be hardware or software fault!</u>

- If hardware,
    1. Input cable misaligned—Realign correctly.
    2. Input module is defective
    3. Further amplifier diagnostics need to be performed—see individual service manuals to troubleshoot.
- If software, verify if input module is not in the MUTED mode on the defective channel by using System Architect software. If not muted, use System Architect software to determine error status.

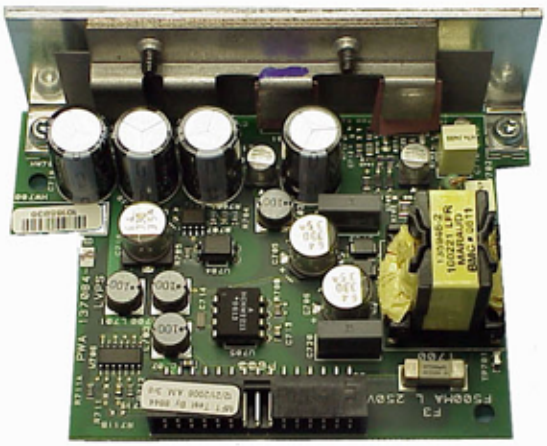
MAIN PCB ASSEMBLIES ON DP1



137084-5AJBL PWA,DP1 MAIN/SMPS



137084-5CJBL LF MOD



137084-5BJBL LVPS